AMENDMENTS TO THE CLAIMS

Please cancel claim 2, and amend claims 1, 3-14, and 22, such that the status of the claims is as follows.

1. (Currently Amended) An integrated circuit wafer comprising:

an integrated circuit die having a device trimming fuse circuit;

a first pad positioned in a scribe lane adjacent the integrated circuit die; ~~and~~

a second pad positioned in the scribe lane adjacent the integrated circuit die;

a first conductor extending from the device trimming fuse circuit to the first pad; and

~~, wherein the integrated circuit is trimmed by selectively applying a signal from the first pad to the fuse circuit through the first conductor.~~

a second conductor extending from the device trimming fuse circuit to the second pad, wherein the first and second conductors form a current path that provides a fuse blowing signal selectively applied between the first pad and the second pad to the device trimming fuse circuit to electrically trim the integrated circuit die.

2. (Canceled)

3. (Currently Amended) The integrated circuit wafer of claim [[2]] 1 wherein the first and second pads are a fuse pad and a supply pad, respectively.

4. (Currently Amended) The integrated circuit wafer of claim 1 wherein the device trimming fuse circuit includes a fuse and circuitry for sensing whether the fuse is blown.

5. (Currently Amended) The integrated circuit of claim [[3]] 4 wherein the fuse and the circuitry are aligned generally parallel to an edge of an integrated circuit die.

6. (Currently Amended) The integrated circuit of claim 5 wherein the first and second conductors [[is]] are oriented generally perpendicular to the edge.

7. (Currently Amended) An integrated circuit wafer comprising:

a plurality of integrated circuit dice separated from one another by scribe lanes, the dice having device trimming fuse circuits adjacent the scribe lanes; and

a plurality of pads positioned in the scribe lane, wherein each device trimming fuse circuit is connected to two of the plurality of pads positioned in the scribe lane ~~and connected to the device trimming fuse circuits~~ by conductors that create a current path that allows ~~for selectively applying~~ a fuse blowing signal to be applied to the device trimming fuse circuits to electrically trim the integrated circuit die, so that following singularization of the dice from the wafer, the pads are disconnected from the device trimming fuse circuits.

8. (Currently Amended) The integrated circuit wafer of claim 7 wherein each device trimming fuse circuit is connected to a fuse pad and a power supply pad.~~the plurality of pads include a fuse pad and a power supply pad connected to each fuse circuit.~~

9. (Currently Amended) The integrated circuit wafer of claim 8 wherein each device trimming fuse circuit includes a fuse connected ~~to~~ between the fuse pad and the power supply pad by the conductors which cross the die edges.

10. (Currently Amended) The integrated circuit wafer of claim 9 wherein each device trimming fuse circuit includes circuitry for sensing whether the fuse is blown.

11. (Currently Amended) The integrated circuit wafer of claim 7 wherein the device trimming fuse circuits are aligned in rows generally parallel to the scribe lanes.

12. (Currently Amended) A trimmable integrated circuit comprising:

a plurality of device trimming fuses positioned adjacent a die edge of the integrated circuit;

a plurality of pads positioned in a scribe lane adjacent to the die edge; and

a plurality of conductors extending across the die edge for connecting at least two of the plurality of pads ~~and~~ to each of the plurality of ~~the~~ device trimming fuses to allow electrical trimming of the integrated circuit by selective blowing of the device trimming fuses, the conductors being severable during singularization of the integrated circuit.

13. (Currently Amended) The trimmable integrated circuit of claim 12 wherein the device trimming fuses are aligned in a row generally parallel to the die edge.

14. (Currently Amended) The trimmable integrated circuit of claim 12 wherein a pair of adjacent device trimming fuses share one common pad.

15.-21. (Canceled)

22. (Currently Amended) An integrated circuit die having a plurality of device trimming fuse circuits adjacent a die edge and conductors extending from the device trimming fuse circuits to the die edge, the conductors providing connection between the device trimming fuse circuits and a plurality of pads located in a scribe lane, the plurality of pads being ~~which are~~ severed from the die subsequent to selective blowing of fuses of the device trimming fuse circuits by applying a signal to a current path that includes two of the plurality of pads and a selected device trimming fuse circuit.